AMENDMENTS TO THE CLAIMS:

If entered, this listing of claims will replace all prior versions and listings of claims in the application.

Listing of Claims:

1. (Original) A method of detecting a reticle option layer in an integrated circuit device comprising:

measuring the current through a first MOS transistor in an integrated circuit device by forcing a test voltage on the drain and the gate wherein said gate and said drain of said first MOS transistor are connected together, wherein the source of said first MOS transistor is connected to a reference voltage, and wherein said first MOS transistor is not parametrically affected by a reticle option layer;

measuring the current through a second MOS transistor in said integrated circuit device by forcing same said test voltage on the drain and the gate wherein said gate and said drain of said second MOS transistor are connected together, wherein the source of said second MOS transistor is connected to a reference voltage, and wherein said

second MOS transistor is parametrically affected by said reticle option layer; and

comparing said current through said first MOS transistor and said current through said second MOS transistor to detect the presence of said reticle option layer in said integrated circuit device.

2. (Original) The method according to Claim 1 wherein said reticle option layer comprises a threshold voltage implantation.

3. (Original) The method according to Claim 1 wherein said reticle option layer comprises one of the group of: polysilicon, metal, and threshold implantation.

4. (Original) The method according to Claim 1 wherein said first MOS transistor and said second MOS transistor are the same size, the same direction and in close proximity.

5. (Original) The method according to Claim 1 wherein said reticle option layer comprises a combination of reticle layers.

6. (Original) The method according to Claim 5 wherein said combination of reticle layers comprises the group of: polysilicon, metal, and threshold implantation.

7. (Original) The method according to Claim 1 wherein said measuring of said current through said first MOS transistor and said measuring of said current through said second MOS transistor is by directly probing the die of said integrated circuit device.

8. (Original) The method according to Claim 1 wherein said measuring of said current through said first MOS transistor and said measuring of said current through said second MOS transistor is by probing an output pin of packaged said integrated circuit device.

9. (Original) The method according to Claim 1 wherein said first MOS transistor and said second MOS transistor comprise one of the group of: NMOS transistors and PMOS transistors.

10. (Previously Presented) A method of detecting a threshold voltage implantation reticle option layer in an integrated circuit device comprising:

measuring the current through a first MOS transistor in an integrated circuit device by forcing a test voltage on the drain and the gate wherein said gate and said drain of said first MOS transistor are connected together, wherein the source of said first MOS transistor is connected to a reference voltage, and wherein said first MOS transistor has a first threshold voltage implantation but not a threshold voltage implantation reticle option layer;

measuring the current through a second MOS transistor in said integrated circuit device by forcing same said test voltage on the drain and the gate wherein said gate and said drain of said second MOS transistor are connected together, wherein the source of said second MOS transistor is connected to a reference voltage, and wherein said second MOS transistor has both said first threshold voltage implantation and said threshold voltage implantation reticle option layer; and

comparing said current through said first MOS transistor and said current through said second MOS transistor to detect the presence of said threshold voltage implantation reticle option layer in said integrated circuit device.

11. (Original) The method according to Claim 10 wherein said first MOS transistor and said second MOS transistor are the same size, the same direction and in close proximity.

12. (Original) The method according to Claim 10 wherein said measuring of said current through said first MOS transistor and said measuring of said current through said second MOS transistor is by directly probing the die of said integrated circuit device.

13. (Original) The method according to Claim 10 wherein said measuring of said current through said first MOS transistor and said measuring of said current through said second MOS transistor is by probing an output pin of packaged said integrated circuit device.

14. (Original) The method according to Claim 10 wherein said first MOS transistor and said second MOS transistor comprise one of the group of: NMOS transistors and PMOS transistors.

15. (Previously Presented) A method of detecting a threshold voltage implantation reticle option layer in an integrated circuit device comprising:

selecting a first NMOS transistor in an integrated circuit device in a first test mode to couple the voltage at the drain and the gate of said first NMOS transistor to an output pin of said integrated circuit device wherein said gate and said drain of said first NMOS transistor are connected together,

wherein the source of said first NMOS transistor is connected to ground, and wherein said first NMOS transistor has a first threshold voltage implantation but not a threshold voltage implantation reticle option layer;

measuring said voltage at said output pin in said first test mode when an internal test voltage is connected to said drain and said gate of said first NMOS transistor through a first internal standard resistance;

selecting a second NMOS transistor in said integrated circuit device in a second test mode to couple the voltage at the drain and the gate of said second NMOS transistor to said output pin of said integrated circuit device wherein said gate and said drain of said second NMOS transistor are connected together,

wherein the source of said NMOS transistor is connected to

ground, and wherein said second NMOS transistor has both said first threshold voltage implantation and said threshold voltage implantation reticle option layer;

measuring said voltage at said output pin in said second test mode when said internal test voltage is connected to said drain and said gate of said second NMOS transistor through a second internal standard resistance; and

comparing said voltage at said output pin in said first test mode with said voltage at said output pin in said second test mode to detect the presence of said threshold voltage implantation reticle option layer in said integrated circuit device.

16. (Original) The method according to Claim 15 wherein said selecting of said first NMOS transistor is by a multiplex circuit and wherein said selecting of said second NMOS is by a multiplex circuit.

17. (Original) The method according to Claim 15 further comprising amplifying said voltage at said drain and said gate of said first NMOS transistor and said second NMOS transistor to thereby generate an amplified drain and gate voltage at said output pin.

18. (Original) The method according to Claim 15 wherein said first NMOS transistor and said second NMOS transistor are the same size, the same layout orientation, and in close proximity.

19. (Original) The method according to Claim 15 wherein said first internal resistance and said second internal resistance comprise the same resistance value.

20. (Previously Presented) A method of detecting a threshold voltage implantation reticle option layer in an integrated circuit device comprising:

selecting a first PMOS transistor in an integrated circuit device in a first test mode to couple the voltage at the drain and the gate of said first PMOS transistor to an output pin of said integrated circuit device wherein said gate and said drain of said first PMOS transistor are connected together, wherein the source of said first PMOS transistor is connected to an internal standard voltage, and wherein said first PMOS transistor has the standard threshold voltage implantation but not the threshold voltage implantation reticle option layer;

measuring said voltage at said output pin in said

first test mode when said drain and said gate of said first PMOS transistor are connected to ground through a first internal standard resistance;

selecting a second PMOS transistor in said integrated circuit device in a second test mode to couple the voltage at the drain and the gate of said second PMOS transistor to said output pin of said integrated circuit device wherein said gate and said drain of said second PMOS transistor are connected together, wherein the source of said second PMOS transistor is connected to said internal standard voltage, and wherein said second PMOS transistor has both said standard threshold voltage implantation and said threshold voltage implantation reticle option layer;

measuring said voltage at said output pin in said second test mode when said drain and said gate of said second PMOS transistor are connected to said ground through a second internal standard resistance; and

comparing said voltage at said output pin in said first test mode with said voltage at said output pin in said second test mode to detect the presence of said threshold voltage implantation reticle option layer in said integrated circuit device.

21. (Original) The method according to Claim 20 wherein said selecting of said first PMOS transistor is by a multiplex circuit and wherein said selecting of said second PMOS is by a multiplex circuit.

22. (Original) The method according to Claim 20 further comprising amplifying said voltage at said drain and said gate of said first PMOS transistor and said second PMOS transistor to thereby generate an amplified drain and gate voltage at said output pin.

23. (Original) The method according to Claim 20 wherein said first PMOS transistor and said second PMOS transistor are the same size, the same layout orientation, and in close proximity.

24. (Original) The method according to Claim 20 wherein said first internal resistance and said second internal resistance comprise the same resistance value.